REMARKS

Discussion of the Cited References

Aram et al. U.S. Patent No 6,400,214 is cited for a 102(b) rejection to claims 1-4, 7-9, 10-14 and 16-20. It is also cited as a primary reference for a 103(a) rejection to claims 5, 6, 14 and 15. Claims 1-9 are cancelled, which render rejections set forth are moot.

Applicants submit that the present invention, as set forth in claims 10 and 19 are neither taught, suggested nor disclosed by Aram '214, or any of the other cited references, taken alone or in combination. As such, claim 10 is submitted new and unobvious over Aram '214 and any of the other cited references, taken alone or in combination, and thus should be allowable. Dependent claims 11-18 and 20 are also submitted to be allowable because of the dependency to allowable independent claims 10 and 19.

Rejections Addressed To Claims 10-18

Claim 10, as amended, recites:

> An analog-to-digital signal converter circuit, comprising:
>
> a first capacitor, having a first terminal and a second terminal, wherein said first terminal is coupled to a first voltage level;
>
> a clock generator, for generating a plurality of clock signals;
>
> a switching capacitor network, coupled to said second terminal of said first capacitor, wherein the switching capacitor network receives an analog signal and said clock signals, *said switching capacitor network stores a portion of charges of said analog signal, and outputs said portion of charges according to said clock signals to charge the first capacitor*, and generates a threshold voltage associated with said first capacitor; and
>
> a comparator, for *comparing said threshold voltage with said analog signal and outputting a digital signal*. (Emphasis added)

Applicants submit that such an analog-to-digital signal converter circuit as set forth in claim 10 is neither taught, suggested nor disclosed by Aram '214, or any of the other cited

references, taken alone or in combination. For the reasons discussed above, Aram '214 fails to teach that "said switching capacitor network stores a portion of charges of said analog signal, and outputs said portion of charges according to said clock signals to charge the first capacitor, ..., and a comparator, for comparing said threshold voltage with said analog signal and outputting a digital signal" that are required for the present invention as set forth in claim 10.

Aram '214 teaches an amplifier 134. However, such an amplifier 134 does not read on the comparator for comparing said threshold voltage with said analog signal and outputting a digital signal as set forth in claim 10. The inputs of the amplifier 134 of Aram '214 are Vref and a signal by the negative feedback from the Vrefp.

However, in the present invention, the comparator compares the threshold voltage with said analog signal and outputting a digital signal. The threshold voltage is generated associated with the first capacitor which is charged by the portion of charges of the analog signal according to said clock signals. Aram '214 fails to teach, disclose or suggest the feature above. Accordingly, independent claim 10 is submitted to be novel, unobvious over Aram '214, or any other of the cited references, taken alone or in combination, and thus should be allowable.

If independent claim 10 is allowable over the prior art of record, then its dependent claims 11-18 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 10. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Rejections Addressed To Claims 19-20

Claim 19, as originally filed, recites:

> A method for converter an analog signal to a digital signal, comprising:
> providing a first capacitor and a plurality of clock signals;
> storing a portion of charges of an analog signal according to said clock signals;
> *generating a threshold voltage according to said clock signals based on said portion of charges associated with said first capacitor* ; and
> *comparing said threshold voltage with said analog signal in order to output a digital signal*. (Emphasis added)

Applicants submit that such an analog-to-digital signal converter circuit as set forth in claim 19 is neither taught, suggested nor disclosed by Aram '214, or any of the other cited references, taken alone or in combination. For the reasons discussed above, Aram '214 fails to teach that "generating a threshold voltage according to said clock signals based on said portion of charges associated with said first capacitor ; and comparing said threshold voltage with said analog signal in order to output a digital signal" that are required for the present invention as set forth in claim 19.

Aram '214 teaches an amplifier 134. However, such an amplifier 134 does not read on "comparing said threshold voltage with said analog signal and outputting a digital signal" as set forth in claim 19. The inputs of the amplifier 134 of Aram '214 are Vref and a signal by the negative feedback from the Vrefp.

However, in the present invention, the threshold voltage is compared with the analog signal and outputting a digital signal. The threshold voltage is generated according to said clock signals based on said portion of charges associated with said first capacitor. Aram '214 fails to teach, disclose or suggest the feature above. Accordingly, independent claim 19 is submitted to be novel, unobvious over Aram '214, or any other of the cited references, taken alone or in combination, and thus should be allowable.

If independent claim 19 is allowable over the prior art of record, then its dependent claim 20 is also allowable as a matter of law.

Customer No.: 31561
Application No.: 10/707,867
Docket No.: 11870-US-PA

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 10-20 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : Jan. 27, 2006

Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw